

PCIe Carrier board of the Arria[®] 10 SoC SoM ORDERING INFORMATION:
RXCA10S0000F34-FHPOSA

With their combination of performance, power efficiency, and compact form factor, Arria 10 devices are ideal for a broad range of applications, including communications, data center, military, broadcast, ...

Arria 10 SoC FPGA System on Module with compact F34 package, featuring 32-bit DDR4 for HPS and optional ECC for enhanced reliability.

The 28.05-Gbps transceivers are ideal for interfacing with the emerging CFP2 and CFP4 optical modules that typically require four lanes at data rates in the range of 25 to 28 Gbps. Backplane ...

Intel Arria 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Arria 10 devices, you must consider the operating ...

Provides an overview of the Arria 10 device family features, ordering codes options, maximum resource counts, and available device packages.

Arria 10 devices support an optional chip-wide output enable that allows you to override all tri-states on the device I/Os. When this DEV_OE pin is driven low, all I/O pins are tri-stated; when this pin is ...

Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.

The module features up to 24 high-speed transceivers operating at up to 17.4 Gbps and extensive I/O (LVDS and single-ended) exposed via high-speed board-to-board connectors, delivering flexible ...

Equipped with up to 48 full-duplex transceivers and a dual-core ARM Cortex-A9 HPS, the Altera[®] Arria[®] 10 SX FPGA provides enhanced capabilities. Explore Altera[®] Arria[®] 10 FPGAs & SoCs, delivering ...

Bank 3B, 3C, 3A supports variable IO level setting from PMIC (1.8V, 1.5V, 1.35V, 1.2V). Each FPGA IO Bank (2A,3A,3B,3C) which goes to Expansion connectors support two General Purpose Clock Input ...

Web: <https://www.busydoniemiecwaldii.pl>